

ABSTRACT OF THE DISCLOSURE

A semiconductor device employs a SESO memory or a phase change memory which has a smaller memory cell area than SRAM. The semiconductor device has a plurality of memory banks each composed of the SESO or phase change memories, and a cache memory which has a number of ways equal to the ratio of a write speed ( $m$ ) to a read speed ( $n$ ). The semiconductor device controls the cache memory such that a write back operation is not repeated on the same memory bank.